REMARKS

Fig. 1 has been amended.

Minor Amendments have been made to independent claims 1-3 and 8-10 to further clarify the present invention. Support for the claim amendments can be found at page 6, lines 1-7, 15-16, and 20-22, for example.

Claims 1-30 are pending and under consideration. Reconsideration is respectfully requested.

Claims 1-3 and 8-10 are independent claims and claims 4-7 and 11-30 depend from claims 1-3 and 8-10 respectively.

Applicants respectfully thank the Examiner for acknowledgment of references cited in the IDS filed on December 14, 2005.

OBJECTION TO THE DRAWINGS:

The heading of Fig. 1 has been amended to recite "Prior Art". Therefore, withdrawal of the objection to the drawings is respectfully requested.

REJECTION OF THE CLAIMS UNDER 35 U.S.C.§102(b):

At page 2 of the Office Action, claims 1-4, 7-11, 14-16, 21-24 and 29-30 were rejected under 35 USC §102(b) as being anticipated by Kubota et al. (U.S. Patent No. 6,437,768; hereinafter referred to as "Kubota"). The foregoing rejection is respectfully traversed.

Claim 1 has been amended to recite:

"A memory device for driving a display panel comprising:
arrays of memory cells storing binary information;
pairs of bit line-bit bar line connected to the memory cells;
first transfer gates connected to one end of the bit line-bit bar line pairs and switched by a column address to access the memory cells;
second transfer gates connected to the other end of bit line-bit bar line pairs and switched to read out the binary information stored in the memory

cells; and

data buffers to receive the read-out binary information of the memory cells from the second transfer gates, by the switching operation of the second transfer gates and to store the read-out binary information,

wherein signals switching the second transfer gates are derived from a single enable signal and divided into several groups, and the signal for each group has a different time delay."

Independent claims 2, 3 and 8-10 have been amended to recite features somewhat similar to those recited in amended claim 1.

The Examiner asserts that Kubota discloses the features of claim 1, for example, in Figs. 1, 3, 6 and 9. The Applicants respectfully disagree with the Examiner's assertion. Specifically, the Applicants assert that Kubota fails to disclose "…first transfer gates connected to one end of the bit line-bit bar line pairs and switched by a column address to access the memory cells; second transfer gates connected to the other end of bit line-bit bar line pairs and switched to read out the binary information stored in the memory cells; and data buffers to receive the read-out binary information of the memory cells from the second transfer gates, by the switching operation of the second transfer gates and to store the read-out binary information, wherein signals switching the second transfer gates are derived from a single enable signal and divided into several groups, and the signal for each group has a different time delay," as recited in amended claim 1, for example.

In contrast, Kubota merely discloses a shift register circuit including a plurality of serially connected latch circuits, for sequentially transmitting a pulse signal in sync with a rising and a falling of a clock signal and an output circuit for sequentially outputting a video signal to data signal lines in sync with the pulse signal outputted from the shift register circuit (see Abstract). The latch circuits are connected in series and divided into groups each having arbitrary stage numbers (see column 7, lines 36-38, for example). Further, Kubota discloses that the stage numbers of the latch circuits in each latch circuit group is set in such a manner to minimize the time different between the output signal from the latch circuit group and the ideal timing of another signal outputted from the output circuit such as a data signal (see column 8, lines 40-45). Thus, the stage numbers of the latch circuits increases with a distance from the input side of the video signal which is inputted into the output circuit as a

data signal. The stage numbers of the latch circuits are determined to minimize the time difference between the pulse signal outputting from each latch circuit and the video signal outputting in sync with the pulse signal.

At pages 3-4 of the Office Action, the Examiner asserts that Kubota discloses the Applicants "first and second transfer gates" as recited in amended claim 1, for example at Fig. 3 thereof. Specifically, the Examiner asserts that the input (IN) and output (OUT) are comparable to the Applicants "first and second transfer gates". The Applicants respectfully disagree with the Examiner. The Applicants respectfully submit that Kubota fails to disclose that the IN terminal shown in Fig. 3 of Kubota is connected to one end of the bit line-bit bar line pairs and switched by a column address to access the memory cells, and that the OUT terminal is connected to the other end of bit line-bit bar line pairs and switched to read out the binary information stored in the memory cells. Nor does Kubota disclose that data buffers receive the read-out binary information of the memory cells from the OUT terminal, by the switching operation of the OUT terminal.

In contrast, Kubota only discloses in column 8, lines 28-39 that the latch circuit in the signal input terminal (IN) side transmits a signal inputted through the IN terminal to another latch circuit in the following stage in sync with the internal clock signal and an inverted signal inputted thereto while outputting the same to the OUT terminal.

Further, Kubota fails to disclose that "signals switching the second transfer gates are derived from a single enable signal and divided into several groups, and the signal for each group has a different time delay," as also recited in amended claim 1. The start signal ST of Kubota is not comparable to the Applicants "signals switching the second transfer gates" as recited in amended claim 1.

The teachings of Kubota are fundamentally different from that of the present invention as recited in amended claim 1, for example. That is, Kubota fails to disclose the Applicants "second transfer gates" and thus fails to provide the advantages of the second transfer gates having different time delay signals in different groups, and reducing the peak current by allowing the data buffers to have different time delay signals in different groups and by allowing the enable signals of

the data buffers and the switching signals of the second transfer gates to have different time delay signals in different groups.

The comments mentioned above may also be applied to the rejection of independent claims 2-3 and 8-10. Further, these comments may also be applied to the rejection of dependent claims 4, 7, 11, 14-16, 21-24 and 29-30 which depend from independent claims 2-3 and 8-10 respectively.

Thus, the present invention as claimed in independent claims 1-3 and 8-10 patentably distinguish over Kubota. Further, dependent claims 4, 7, 11, 14-16, 21-24 and 29-30 also patentably distinguish over Kubota, at least based on their dependency upon claims 1-3 and 8-10.

Accordingly, withdrawal of the 102(b) rejection of these claims is respectfully requested.

REJECTION OF THE CLAIMS UNDER 35 U.S.C.§103(a):

At page 5 of the Office Action, claims 5, 6, 12, 13, 17-20 and 25-28 were rejected under 35 U.S.C. 103(a) as being unpatentable over Kubota. The foregoing rejection is respectfully traversed.

Claims 5, 6, 12, 13, 17-20 and 25-28 respectively depend from claims 1-3 and 8-10, therefore, the comments mentioned above may also be applied to the rejection of these claims.

Further, claims 5, 6, 12, 13, 17-20 and 25-28 disclose patentably distinguishing features of their own. For example, claim 6 recites: “the first transfer gates are switched by the column address as being grouped by unit of 2^n, wherein n is a positive integer including 0.

At pages 5 and 6 of the Office Action, the Examiner admits that Kubota fails to disclose all of the features recited in claims 5, 6, 12, 13, 17-20 and 25-28 and attempts to take Official Notice regarding the deficiencies thereof. The Applicants respectfully traversed the Examiner’s assertion of obviousness and Official Notice

and request that the Examiner either withdraw the 103(a) rejection of these claims over Kubota or provide a reference(s) to support this assertion.

Thus, the Applicants respectfully submit that Kubota alone fails to establish a prima facie case of obviousness over the present invention as claimed. Accordingly, withdrawal of the 103(a) rejection is respectfully requested.

CONCLUSION:

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

Respectfully submitted,

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